In the Claims:

Amend claims 1, 8, 11, 13, 22 and 30 to read as follows:

B1

1. (Amended) A method of generating a clock signal on an integrated circuit (IC), the method comprising the steps of:

generating a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal; and

generating a clock signal from the differential pair for the IC by employing both the first sinusoidal signal and the second sinusoidal signal to form the clock signal.

B2

8. (Amended) A method of driving a clock tree on an integrated circuit (IC), the method comprising the steps of:

providing an IC having a clock tree;

distributing a clock signal in the form of a differential sinusoidal signal pair in a portion of the clock tree, the differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal; and

generating a local clock signal from the differential pair by employing both the first sinusoidal signal and the second sinusoidal signal to form the local clock signal.

B3

11. (Amended) The method of claim 8, wherein generating the local clock signal includes using a differential amplifier.

B4

13. (Twice amended) A clock circuit for an IC, comprising:

a generating circuit adapted to generate a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal;

a distribution circuit coupled to the generating circuit and adapted to distribute the differential sinusoidal signal pair on the IC; and

B4

a plurality of clock receiver circuits coupled to the distribution circuit and adapted to convert the differential sinusoidal signal pair into respective local clock signals by employing both the first sinusoidal signal and the second sinusoidal signal to form each local clock signal.

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22. (Amended) Apparatus for generating and distributing a clock signal, comprising:

B5

means for generating a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal;

means for distributing the generated differential sinusoidal signal pair; and

means for receiving the distributed differential sinusoidal signal pair and generating a local clock signal from the received differential sinusoidal signal pair by employing both the first sinusoidal signal and the second sinusoidal signal to form the local clock signal.

B6

30. (Amended) The apparatus of claim 22, wherein the means for receiving and generating includes a differential amplifier.

Add new claims 31-34 as below.

B7

31. (New) A method of generating a clock signal on an integrated circuit (IC), the method comprising the steps of:

generating a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal; and

generating a clock signal from the differential pair for the IC by subtracting the first sinusoidal signal from the second sinusoidal signal.

32. (New) A method of driving a clock tree on an integrated circuit (IC), the method comprising the steps of:

providing an IC having a clock tree;

distributing a clock signal in the form of a differential sinusoidal signal pair in a portion of the clock tree, the differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal; and

generating a local clock signal from the differential pair by subtracting the first sinusoidal signal from the second sinusoidal signal.

33. (New) A clock circuit for an IC, comprising:

a generating circuit adapted to generate a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal;

a distribution circuit coupled to the generating circuit and adapted to distribute the differential sinusoidal signal pair on the IC; and

a plurality of clock receiver circuits coupled to the distribution circuit and adapted to convert the differential sinusoidal signal pair into respective local clock signals by subtracting the first sinusoidal signal from the second sinusoidal signal.

34. (New) Apparatus for generating and distributing a clock signal, comprising:

means for generating a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal;

BY

means for distributing the generated differential sinusoidal signal pair; and

means for receiving the distributed differential sinusoidal signal pair and generating a local clock signal from the received differential sinusoidal signal pair by subtracting the first sinusoidal signal from the second sinusoidal signal.

REMARKS

To remove the finality of the pending Office Action and to obtain consideration of the above-indicated claim amendments, a Request for Continued Examination is filed herewith, together with the requisite fee.

Claims 1-34 are now in this application, new claims 31-34 having been added in this paper. Claims 1-30 stand rejected and are now presented for reconsideration in view of the foregoing amendments and the following remarks.

Claims 1-30 were "rejected under 35 USC §103(a) as being unpatentable over the Wissell et al. reference".

The rejected independent claims, namely claims 1, 8, 13 and 22, have been amended to overcome this rejection. Claim 1, as now presented, is directed to a "method of generating a clock signal on an integrated circuit (IC)". Claim 1 recites "generating a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal" and "generating a clock signal from the